A5 SCHEDULE	1999																2000																					
EE-441 / EE-442	September				October					November				December				January				February				March				April							
Stereo Amplifier/Tur	5	#	#	#	3	#	#	#	#	7	#	#	#	5	#	#	#	2	9	#	#	#	6	#	#	#	5	#	#	#	2	9	#	#	30		
System Design (KRL)		oo	oo	oo	oo	oo																															
Specs / Interface Rqmts. (KRL)						■																															
Switching Matrix Design (PDF)							oo	oo	oo	oo	oo																										
Multiplexer (PDF)							oo																														
Preamp (KRL)								oo																													
Equalizer (JVdS)									oo	oo	oo																										
Treble (JVdS)									oo																												
Mid-Band (JVdS)										oo																											
Bass (JVdS)											oo																										
Power Amplifier Design (KRL)												oo	oo	oo					oo	oo	oo	oo	oo	oo	oo												
Driver (KRL)												oo																									
Intermediate Power Amp (PDF)													oo	oo																							
Power Amp (JVdS)																			oo	oo	oo	o															
Feedback Loop (JVdS)																						o	oo	oo													
AM/FM Tuner Design (JVdS)							oo	oo	oo	oo	oo	oo	oo	oo					oo	oo	oo	oo	oo	oo													
FM IF Amplifier/Demod. (JVdS)							oo	oo	oo	oo	oo																										
Frequency Synthesizer (KRL)												oo	oo	oo					oo																		
AM IF Amplifier/Demod. (PDF)																				oo	oo																
FM Preamp (KRL)																						oo															
Antennas (AM and FM) (PDF)																							oo	oo													
Control Logic (KRL)							oo	oo	oo	oo	oo	oo							oo	oo	oo	oo	oo	oo													
Display (KRL)													oo	oo																							
Define Requirements (KRL)													oo	o																							
Write Purchase Order (PDF)														■																							
Power Supply Design (KRL)																			oo	oo	oo	oo	oo	oo	oo												
+ 30 VDC (KRL)																			oo	oo																	
+ 5 VDC (KRL)																					oo	oo															
- 5 VDC (KRL)																							oo														
Integrate PS Modules (JVdS)																								oo	oo												
System Integration (PDF)																										oo		oo	oo	oo	oo	oo	oo	oo			
Integrate (PDF)																												oo									
System Functional (KRL)																										oo											
Characterize (JVdS)																										oo		oo	oo								
Optimize (Redesign) (KRL)																													oo	oo	oo	oo					
Final Data (PDF)																															oo	oo	oo	oo	oo		
Demo Day (KRL)																																		■			