

SCHEDULE UPDATE (Oct. 24)	1999												2000																						
	September				October				November				December				January			February			March			April									
	5	#	#	#	3	#	#	#	7	#	#	#	5	#	#	#	2	9	#	#	#	6	#	#	#	5	#	#	#	2	9	#	#	30	
Stereo Amplifier/Tur																																			
System Design (KRL)	XX	XX	XX	XX	XX	XX																													
Specs / Interface Rqmts. (KRL)					■																														
Switching Matrix Design (PDF)						XX	XX	oo	oo	oo	ss																								
Multiplexer (PDF)						XX																													
Preamp (KRL)						XX	ss																												
Equalizer (JVdS)								oo	oo	oo	ss																								
Treble (JVdS)								oo	ss																										
Mid-Band (JVdS)									oo	ss																									
Bass (JVdS)										oo	ss																								
Power Amplifier Design (PDF)										oo	oo	oo	ss				oo	oo	oo	oo	oo	oo	oo												
Driver (KRL)										oo	ss																								
Intermediate Power Amp (PDF)											oo	oo	ss																						
Power Amp (JVdS)																	oo	oo	oo	o															
Feedback Loop (JVdS)																				o	oo	oo													
AM/FM Tuner Design (JVdS)						XX	XX	oo	oo	oo	oo	oo	oo				oo	oo	oo	oo	oo	oo	oo												
FM IF Amplifier/Demod. (JVdS)						XX	XX	oo	oo	oo																									
Frequency Synthesizer (KRL)										oo	oo	oo					oo																		
AM IF Amplifier/Demod. (PDF)																	oo	oo																	
FM Preamp (KRL)																			oo																
Antennas (AM and FM) (PDF)																				oo	oo														
Control Logic (KRL)						XX	XX	XX	XX	oo	oo						oo	oo	oo	oo	oo	oo	oo												
Display (KRL)										oo	oo																								
Define Requirements (KRL)										oo	o																								
Write Purchase Order (PDF)											■																								
Power Supply Design (KRL)																	oo	oo	oo	oo	oo	oo	oo												
+ 30 VDC (KRL)																	oo	oo																	
+ 5 VDC (KRL)																		oo	oo																
- 5 VDC (KRL)																			oo																
Integrate PS Modules (JVdS)																				oo	oo														
System Integration (PDF)																						oo	oo			oo	oo	oo	oo	oo	oo				
Integrate (PDF)																						oo	oo												
System Functional (KRL)																						oo													
Characterize (JVdS)																						oo				oo	oo								
Optimize (Redesign) (KRL)																										oo	oo	oo							
Final Data (PDF)																											oo	oo	oo	oo					
Demo Day (KRL)																														■					