“TURNING DARK SILICON INTO GREEN THROUGH ULTRA ENERGY-EFFICIENT VLSI CIRCUITS - FROM NANO TO MACRO SCALE”

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Wu and Chen Auditorium, 3:00 – 4:00pm

Abstract
In the last few years, evolution of CMOS VLSI circuits has significantly departed from the historical Dennard’s scaling trends. The multi-core era promises sustainable technology scaling thanks to a more efficient utilization of energy. Unfortunately, very recent projections show that multi-core scaling will come to an end in a relatively short amount of time (less than 5 years), since inadequate energy efficiency makes it impossible to fully utilize all the devices available in a chip. The increasing fraction of circuits that cannot be used at the same time in the same chip (“dark silicon”) will eventually nullify the benefits brought by the exponential increase in transistors per chip as per Moore’s law.

In this talk, the “dark silicon” issue is put into the broad perspective of computing and sensing platforms expanding towards the nano (ubiquitous computing/sensing) and the macro scale (cloud computing). The “turn dark silicon into green silicon”, thus postponing the end of the CMOS scaling era. At nano scale, new ideas and methodologies are discussed to demonstrate the feasibility of ultra-compact sensing/computing platforms (e.g., active RFIDs) with perpetual operation. At macro scale, innovative methodologies and circuit topologies to reduce the consumption of energy-hungry clock domains in high-performance microprocessors (e.g., for servers) will be introduced. At intermediate “meso scale” of portable and mobile electronics, the concept of user experience-driven energy scaling is explored under a case study (near-threshold SRAM memories). Finally, new directions to “turn dark into green silicon” will be openly discussed to provide a long-term perspective on this grand challenge and the related solutions.

Biography
Massimo Alioto is Associate Professor of Electronics at the University of Siena since 2006. He was a Visiting Faculty at EPFL (Switzerland) in 2007, at BWRC – UC Berkeley in 2009-2011, and currently at University of Michigan to work on ultra-energy efficient and resilient computing.

He has authored or co-authored about 170 publications on journals (60, mostly IEEE Transactions) and conference proceedings. He is co-author of the book Model and Design of Bipolar and MOS Current-Mode Logic: CML, ECL and SCL Digital Circuits (Springer, 2005). His primary research interests include ultra low-power circuits for ubiquitous computing and self-powered sensor nodes, active techniques for resilient energy-efficient computing and timing speculation, leakage- and variability-aware design methodologies, circuit techniques in emerging technologies and ultra-low power/area/design cost schemes for information security. He is the director of the Electronics Lab at University of Siena (site of Arezzo).

Prof. Alioto is an IEEE Senior Member and a member of the MuSyC FCRP Center. He is Chair of the “VLSI Systems and Applications” Technical Committee of IEEE CAS Society, and was Distinguished Lecturer in 2009-2010. He has served as Track Chair for a number of conferences (ICCD, ISCAS, ICECS, ICM…) and Technical Program Chair for ICM 2010 and NEWCAS 2012. He currently serves as Associate Editor of eight journals, including the IEEE Transactions on VLSI Systems, the ACM Transactions on Design Automation of Electronic Systems, IEEE Transactions on Circuits – part I.

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